

**CLAIMS**

1. Apparatus for use in a computer system comprising:

5 a pipeline bus architecture, in which data traverses the bus architecture over a plurality of system clock cycles;

a plurality of modules connected to the bus architecture;

wherein the bus architecture comprises:

10 a plurality of bus connection units; and

a plurality of bus portions arranged in series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus connecting unit,

15 wherein each of the modules is connected to the bus architecture by way of a respective one of the bus connection units, and

each of the bus connection units including multiplexer circuitry for selectively connecting a module to the bus architecture.

20 2. Apparatus as claimed in claim 1, wherein each bus connection unit includes output circuitry connected to the bus portions to which the unit is connected, the output circuitry being optimised for the length of the bus portions concerned.

3. Apparatus as claimed in claim 1, wherein the bus portions are all equal in length.

30 4. Apparatus as claimed in claim 1, wherein the pipeline bus architecture comprises a primary pipelined bus and a secondary pipelined bus, the primary and secondary buses being interconnected by an interface, a first plurality of modules connected to the primary bus by means

of respective said bus connection units, and a second plurality of modules connected to the secondary bus by means of respective said bus connection units.

5        5.    Apparatus as claimed in claim 1, wherein a central arbitration unit arbitrates between the modules in order to grant access to the bus architecture.

6.    Apparatus as claimed claim 5, wherein the pipelined bus architecture comprises a primary pipelined bus and a secondary pipelined bus, the primary and  
10    secondary buses interconnected by an interface, a first plurality of modules connected to the primary bus by means of respective said bus connection units, and a second plurality of modules connected to the secondary bus by means of respective said bus connection units.

15        7.    Apparatus as claimed in claim 4, wherein the first plurality of modules are latency intolerant and the second plurality of modules are latency tolerant.

8.    Apparatus as claimed in claim 4, wherein the primary bus is one pipeline stage, as herein defined, in  
20    length.

9.    Apparatus as claimed in claim 1, wherein transactions involving data in excess of a predetermined size are split into a plurality of data packets of fixed size, said packets being independently arbitrated.

25        10.   Apparatus as claimed in any claim 1 comprising separate read, write and transaction buses.

11.   Apparatus as claimed in claim 1, wherein the bus architecture has a width sufficient to permit read and write request transactions to alternate in successive  
30    system clock cycles.

12.   A computer system comprising apparatus as claimed in claim 1.